Reconfigurable Computing:
From Satellites to Supercomputers

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Outline

- Motivations, challenges, vision
- A new national research center
- Selected case studies
- Conclusions
Motivations, Challenges, Vision
Opportunities for HPRC?

From Satellites to Supercomputers!
What is a Reconfigurable Computer?

- System capable of changing hardware structure to address application demands
  - Static or dynamic reconfiguration
  - Reconfigurable computing, configurable computing, custom computing, adaptive computing, etc.
  - Often a mix of conventional & reconfigurable processing technologies (control-flow, data-flow)

- Enabling technology?
  - Field-programmable hardware (FPLDs)

- Applications?
  - Broad range – satellites to supercomputers!
  - Faster, smaller, cheaper, less power & heat, more versatile
When and where do we need RC?

**When do we need RC?**

- When performance & versatility are critical
  - Hardware gates targeted to application-specific requirements
  - System mission or applications change over time
- When the environment is restrictive
  - Limited power, weight, area, volume, etc.
  - Limited communications bandwidth for work offload
- When autonomy and adaptivity are paramount

**Where do we need RC?**

- In conventional HPC systems & clusters where apps amenable
  - Field-programmable hardware fits many demands (but certainly not all)
  - High DOP, finer grain, direct dataflow mapping, bit manipulation, selectable precision, direct control over H/W (e.g. perf. vs. power)
- In space, air, sea, undersea, and ground systems (HPEC)
  - Embedded & deployable systems can reap many advantages w/ RC
Vision for HPRC

- Next frontier for high-speed computing
  - Based on new & emerging technologies in field-programmable hardware
  - Versatility of the CPU, horsepower of the ASIC, adaptive tradeoffs
  - Dual-paradigm computing – conventional and RC processing in tandem
  - Powerful approach for new performance levels in HPC
  - Versatile approach for high-speed embedded computing

- Major research & technology challenges in realizing full potential
  - Vertical gap between users and systems (semantics, productivity)
  - Horizontal gap between conventional and RC processing (architecture)
  - Infrastructure for HPC and HPEC environments (libraries & services)
  - Methods, standards, & tools for application/core portability (reuse)
  - Insight to influence next-generation FPLDs & systems (better targets)

- Many challenges best addressed via industry/university collaboration
  - Industry, government, & academe partners; linkage to standards groups
Bridging the Gaps

**Vertical Gap**
- Semantic gap between design levels
  - Application design by scientists & programmers
  - Hardware design by electrical & computer engineers
- We must bridge this gap to achieve success
  - Better languages and environments to express parallelism of multiple types and at multiple levels
  - Better translators, libraries, run-time systems, target devices
  - Both evolutionary and revolutionary steps
- Finding best balance of **performance**, **productivity**, **portability**

**Horizontal Gap**
- Architectures crossing the processing paradigms
  - Cohesive, optimal collage of CPUs, FPGAs, interconnects, memory hierarchies, communications, storage, et al.
  - Simple retrofit to conventional architecture? Future integration?
Traditional Computing Lessons?

- **Good News**
  - User programming model moved from ML (SDL?) to HLL 😊
    - **Productivity** (abstraction), **portability** (device-independent)
  - CPUs redesigned as better targets; ISA convergence 😊
    - **Performance** (ILP arch tailored for compilers), **portability** (x86)
  - Body of experience incorporated into opt. compilers 😊
    - **Performance** (transparent to user; **productivity** & **portability**)

- **Bad News**
  - Much easier for sequential programming than parallel 😞
    - ILP heavily/transparently mined by device (pipelining, superscalar)
    - Witness major concerns re: multicore/multithreaded apps
  - Mythical parallelizing compilers 😞
    - Complexities of parallel apps & archs beyond modern compilers
    - HPC languages aid design but fail in automating/parallelizing
    - Situation for HPRC is potentially more difficult to automate
A Research Challenge Stack

- **Performance prediction**
  - When and where to exploit RC?

- **Performance analysis**
  - How to optimize complex systems and apps?

- **Numerical analysis**
  - Must we throw DP floats at every problem?

- **Programming languages & compilers**
  - How to productively express & achieve parallelism?

- **System services**
  - How to support variety of run-time needs?

- **Portable core libraries**
  - Where cometh building blocks?

- **System architectures**
  - How to scalably feed hungry FPGAs?

- **Device architectures**
  - How will/must FPLD roadmaps track for HPC or HPEC?
Logistical Challenges

- Fragmented & proprietary set of vendor products
  - Natural for any emerging technology
  - Disconcerting for all but early adopters, risk takers

- C⁴ needed for ultimate success
  - Commitment, cooperation, collaboration, convergence

- Consortia and other partnerships are vital
  - Research consortia: academia + industry + government
    - e.g. NSF Center for High-Performance Reconfigurable Computing (CHREC)
  - Consortia for standards, practices, adoption
    - e.g. OpenFPGA
  - Catalytic initiatives, focused R&D teams
    - e.g. proposed new DARPA program on FPGA tools
A New National Research Center
What is CHREC?

- NSF Center for High-Performance Reconfigurable Computing
  - Pronounced “shreck” 😊
  - Under development since Q4 of 2004 (LOI to NSF)
    - Lead institution grant by NSF to Florida awarded on 09/05/06
    - Partner institution grant by NSF to GWU awarded on 12/04/06
    - BYU and VT hopeful of partner institution grants in Q4 of 2007
  - Kickoff workshop held in Dec’06; CHREC operations began in Jan’07

- Under auspices of I/UCRC Program at NSF
  - Industry/University Cooperative Research Center
    - CHREC is supported by CISE & Engineering Directorates @ NSF
  - CHREC is both a Center and a Research Consortium
    - University groups form the research base (faculty, students)
    - Industry & government organizations are research partners, sponsors, collaborators, and technology-transfer recipients
NSF’s Model for I/UCRC Centers

Research Interaction

University

I/U Centers

Industry

Basic

Applied/Development
Objectives for CHREC

- Serve as first national research center in reconfigurable high-performance computing
  - Basis for long-term partnership and collaboration amongst industry, academe, and government; a research consortium
  - RC: from supercomputers to high-speed embedded systems

- Directly support research needs of our Center members
  - Highly cost-effective manner with pooled, leveraged resources and maximized synergy

- Enhance educational experience for a large set of high-quality graduate and undergraduate students
  - Ideal recruits after graduation for Center members

- Advance knowledge and technologies in this field
  - Commercial relevance ensured with rapid technology transfer
CHREC Faculty

- University of Florida
  - Dr. Alan D. George, Professor of ECE – UF Site Director
  - Dr. Herman Lam, Associate Professor of ECE
  - Dr. K. Clint Slatton, Assistant Professor of ECE and CCE
  - Dr. Greg Stitt, Assistant Professor of ECE
  - Dr. Ann Gordon-Ross, Assistant Professor of ECE
  - Dr. Saumil Merchant, Research Scientist in ECE

- George Washington University
  - Dr. Tarek El-Ghazawi, Professor of ECE – GWU Site Director
  - Dr. Ivan Gonzalez, Research Scientist in ECE
  - Dr. Mohamed Taher, Research Scientist in ECE

- Brigham Young University – pending approval by NSF
  - Dr. Brent E. Nelson, Professor of ECE – BYU Site Director
  - Dr. Michael J. Wirthlin, Associate Professor of ECE
  - Dr. Brad L. Hutchings, Professor of ECE

- Virginia Tech – pending approval by NSF
  - Dr. Shawn A. Bohner, Associate Professor of CS – VT Site Director
  - Dr. Peter Athanas, Professor of ECE
  - Dr. Wu-Chun Feng, Associate Professor of CS and ECE
  - Dr. Francis K.H. Quek, Professor of CS
21 Founding Members in CHREC

- Air Force Research Laboratory
- Altera
- Arctic Region Supercomputing Center
- Cadence
- Hewlett-Packard
- Honeywell
- IBM Research
- Intel
- NASA Goddard Space Flight Center
- NASA Langley Research Center
- NASA Marshall Space Flight Center
- National Cancer Institute & SAIC
- National Reconnaissance Office
- National Security Agency
- Oak Ridge National Laboratory
- Office of Naval Research
- Raytheon
- Rockwell Collins
- Sandia National Laboratories
- Silicon Graphics Inc.
- Smiths Aerospace (now GE Aviation)
Benefits of Center Membership

- **Research and collaboration**
  - Selection of project topics that membership resources support
  - Direct influence over cutting-edge research of prime interest
  - Review of results on semiannual formal basis & continual informal basis
  - Rapid transfer of results and IP from projects @ ALL sites of CHREC

- **Leveraging and synergy**
  - Highly leveraged and synergistic pool of funding resources
  - Cost-effective R&D in today’s budget-tight environment

- **Multi-member collaboration**
  - Many benefits between members
  - e.g. new industrial partnerships & teaming opportunities

- **Personnel**
  - Access to strong cadre of faculty, students, post-docs

- **Recruitment**
  - Strong pool of students with experience on industry & govt. R&D issues

- **Facilities**
  - Access to university research labs with world-class facilities
Education & Outreach

- CHREC is enabling advancements at all its sites
  - New & updated courses
  - Degree curricula enhancements
  - Student internship connections
  - Visiting scholars

**Example:** new RC courses at Florida site
- New undergraduate (EEL4930) & graduate (EEL5934) courses in RC starting Aug’07
  - Lectures, lab experiments, research projects
    - Fundamental topics
    - Special topics from research in CHREC
  - Supported by new RC teaching cluster
    - Sponsored by educational grants from Rockwell Collins & Altera
    - 12 workstations each housing PCIe card with Stratix-II FPGA
Selected Case Studies

1) Simulative Performance Prediction
2) Performance Analysis
3) Applications Studies
4) Device Architectures & Tradeoffs
5) Advanced Space Computing
6) DARPA Study on FPGA Tools
1) Simulative Performance Prediction

Goals
- Develop framework for simulative performance prediction of complex RC systems and apps
  - Facilitate fast system design tradeoffs
- Explore design tradeoffs of complex, multi-paradigm systems & applications via modeling and simulation

Challenges
- Design a framework to accurately model a wide range of current and future RC systems and applications
  - Balance simulation speed and fidelity

Simulation Framework
- Framework divided into two domains
  - Application domain and simulation domain
- Framework allows arbitrary applications to be simulated on any arbitrary system
  - Model components & application scripts can be reused after initial development for rapid simulative analyses
Results Highlights

- Performance prediction from RC system models driven by RC application scripts
  - Scripts characterize high-level behavior of application through defining key events
  - Simulation speed balanced by abstracting away fine computation details

- Results from case study with Hyperspectral Imaging (HSI) illustrate framework capabilities
  - Analyze performance while varying numerous independent variables

Sample RC Application Script

```plaintext
#Sample Script
RC_INITFABRIC 1 55296 100.0E6
RC_CORECONFIG 1 Classify 3.84E6 200 1041 50000 8192 128 0 5000

#initialization
MPI_Init
COMP 288.4118587 685880122 10850480 3147074

MPI_send 0 1 MPI_INT 33554432 1 42
MPI_Recv 1 0 MPI_INT 1048576 1 43

#Loop of processing iterations on FPGA
RC_STARTLOOP 32768
RC_COREREQUEST 1 Classify 8192 0
COMP 15.4
RC_STOPLOOP
COMP 10360.0143
MPI_Recv 1 0 MPI_INT 2097152 1 91
COMP 9821.73

#Wrap up
MPI_Barrier 0 1 MPI_CHAR 64 1 11
MPI_Finalize
```

Projected speedup (vs. 3 GHz Xeon) on cluster of XD1000 servers [EP2S180 FPGA via HT] (left) and cluster of Xeon servers [V4LX100 FPGA via PCI-X] (right)
2) Performance Analysis

- **Goals**
  - **Productively** identify & remedy performance bottlenecks in RC applications (CPUs & FPGAs)

- **Motivations**
  - Complex systems difficult to analyze by hand
    - Manual instrumentation is unwieldy
    - Large volume of raw data is overwhelming
  - Tools to quickly locate performance problems
    - Collect & view performance data with little effort
    - Analyze performance data, identify bottlenecks
    - Critical for complex apps & systems in HPRC

- **Challenges**
  - How do we expand notion of software performance analysis into software-hardware realm of RC?
  - What are common bottlenecks for dual-paradigm applications?
  - What techniques are necessary to detect performance bottlenecks?
  - How do we analyze and present these bottlenecks to a user?
What to Instrument in Hardware?

- **Control**
  - Watch state machines, pipelines, etc.
- **Replicated cores**
  - Understand distribution and parallelism inside FPGA
- **Communication**
  - On-chip (Components, Block RAMs, embedded processors)
  - On-board (On-board memory, other on-board FPGAs or processors)
  - Off-board (CPUs, off-board FPGAs, main memory)

More on this research will be presented at RSSI’07 on Friday by Seth Koehler, UF doctoral student
3) Applications Studies

- Goals
  - Develop understanding from case-study experience of decomposition & mapping strategies w/ complex apps
    - Scenario applications defined jointly with CHREC members
    - Hardware/software partitioning, co-design, optimization
  - Concomitantly explore complimentary issues (HLL vs. HDL, design portability, numerical precision, etc.)

- Motivations
  - HPRC still in its infancy; need more lessons learned & insight w/ real apps

- Research Challenges
  - Multilevel algorithm partitioning, analysis, & optimization
  - Balancing performance with portability, precision, productivity

- Current Activities
  - Application design and evaluation
    - PDF estimation, LIDAR processing, multiscale data fusion, molecular dynamics
  - Development of RC-Amenability test (RAT), a simple speedup predictor
  - Design comparisons (HDL vs. HLL for same app)
    - e.g. LIDAR processing via AccelDSP vs. VHDL, molecular dynamics in Impulse C
Ex: Probability Density Function (PDF) Estimation

- **Background**
  - Compute-intensive problem with wide range of apps (e.g. image proc., machine learning)
  - Case study for RAT (RC Amenability Test) – our methodology for quickly & efficiently estimating speedup of a specific top-level app design on a specific FPGA platform

- **Target platform** – Xeon server hosting Nallatech H101-PCIXM card with V4LX100 FPGA and PCI-X interconnect

<table>
<thead>
<tr>
<th>2-D PDF</th>
<th>Resource utilization (kernels/core =8; BRAM = 512 words)</th>
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<tbody>
<tr>
<td>DSP48s</td>
<td>16/96 16%</td>
</tr>
<tr>
<td>BRAM</td>
<td>36/240 15%</td>
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<tr>
<td>Slices</td>
<td>7272/49152 14%</td>
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RAT prediction

<table>
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<tr>
<th>Predicted Speedup</th>
<th>6.8</th>
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Error analysis

| Max. % Error      | 0.12% |

**1st Board Implementation**

- Speedup (single core) = \( \frac{t_{soft} \text{ (sec)}}{t_{RC} \text{ (sec)}} = \frac{158.75}{34.57} = 4.6 \)

\( t_{soft} \) was computed in C on a 3.2GHz Intel Xeon processor and single-precision floating point

\( t_{RC} \) observed from first board implementation (90 MHz)

- Designed a scalable architecture for higher-dimensional PDF estimation & identified key design parameters
- Investigating portability issues & formulating a design pattern as reference solution for future problems

*Necessity is the mother of invention.*

![2-D Numerical Precision Estimate](image-url)

- 32-bit fixed
- 64-bit float

**Left:** FPGA Estimate

**Right:** GPP Estimate (double)

- Multi-core designs are underway
- Dual-core speedup prediction ~ 15x
4) Device Architectures & Tradeoffs

- Goals: develop fundamental research foundation for comparative analysis and insight on RC & competing processing technologies
  - Study FPLD processing technologies (FPGA, FPOA, et al.), compare vs. alternatives
  - Develop models to quantitatively compare (speed, power)
  - Set stage to later explore new FPLD architectures to serve needs of key apps

- Motivations: comprehensive tradeoff analysis to determine a notional future roadmap for FPLDs to target needs of RC for HPEC and/or HPC

- Challenges
  - Application & kernel benchmarking on disparate suite of devices
    - Broad and complex range of design tools, architecture skills, etc.
  - Analytical modeling of resource, performance, & power characteristics; testbed experimentation to calibrate models

- Approach
  - Evaluate various RC & competing processing technologies
    - Altera Stratix-II/III FPGAs, Xilinx Virtex-4/5 FPGAs, MathStar FPOA, Monarch PCA, Cell Broadband Engine, AltiVec vector accelerator, PowerPC baseline (perhaps GPU in future)
  - Analyze benchmark results, formulate characterization methods, construct device characterization matrix & models => insight on key app/device mappings & tradeoffs
Preliminary Results

- **Characterization Studies**
  - Example: Computational Density
    - **Altera Stratix-II EP2S180**
      - Die area: 40mm x 40mm
      - Process Technology: 90 nm
      - Operations: 2.2 million/cycle
      - Frequency: 450 MHz
      - $\gamma = 1,180$
  - Broader suite of studies (e.g. Device Memory Bandwidth, Computational Intensity, etc.) is underway

- **Kernel Benchmarking**
  - Example: 2D Convolution
    - Using HPEC Challenge benchmarks et al. and retargeting them for devices under study

Note on Cell: multithreaded x6, not vectorized, on SPES; best case projected @ 3.7x4.4 = ~16x speedup

2D convolution specs: 8-bit signed integer numerics, 8-bit pixels, 3x3 mask size, 32Kx1K (32 MB) image size, sharpening filter
5) Advanced Space Computing

What is advanced space computing?
- New concepts, methods, and technologies to enable and deploy high-performance computing in space – for an increasing variety of missions and applications

Why is advanced space computing vital?
- **On-board data processing**
  - Downlink bandwidth to Earth is extremely limited
  - Sensor data rates, resolutions, and modes are dramatically increasing
  - Remote data processing from Earth is no longer viable
  - Must process sensor data where it is captured, then downlink results
- **On-board autonomous processing & control**
  - Remote control from Earth is often not viable
  - Propagation delays and bandwidth limits are insurmountable
  - Space vehicles and space-delivered vehicles require autonomy
  - Autonomy requires high-speed computing for decision-making

Why is it difficult to achieve?
- **Cannot simply strap a rocket to a Cray 😊**
  - Hazardous radiation environment in space
  - Platforms with limited power, weight, size, cooling, etc.
  - Traditional space processing technologies (RadHard) are severely limited
- **Potential for long mission times with diverse set of needs**
  - Need powerful yet adaptive technologies
**Example: NASA/Honeywell/UF Project**

- **1st Space Supercomputer**
  - In-situ sensor processing
  - Autonomous control
  - Speedups of $100 \times$ to $1000 \times$
  - First fault-tolerant, parallel, reconfigurable computer for space (NMP ST-8 orbit in 2009)

- **Infrastructure for fault-tolerant, high-speed computing in space**
  - Robust system services
  - Fault-tolerant MPI services
  - FPGA services
  - Application services
  - Standard design framework
  - Providing transparent API to various resources for earth & space scientists

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**Dependable Multiprocessor (DM)**
Dependable Multiprocessor

DM System Architecture

- System controllers/managers
  - Redundant RadHard PPC boards
- Data processing engines
  - COTS boards (PPC, FPGA, AltiVec)
- Fault-tolerant (FT) infrastructure
  - Versatile dynamic mix
  - SIFT, NMR, ABFT, hybrid

DM Middleware (DMM)

- FT embedded MPI (FEMPI)
- FT system services
- HA middleware
- Apps & FPGA services
Dependable Multiprocessor

- **Space Missions for DM**
  - First is NMP ST-8 mission in 2009 for NASA/JPL
    - 6-month orbit, minimal configuration, technology proof of concept
    - HPRC system, but stripped (PPC clocks slowed, FPGAs removed, data network downgraded, etc.) to save cost, weight, power for test mission
  - Many potential opportunities for DM deployment & HPRC in space
    - Upcoming NASA missions and apps in space, such as:
      - Hubble Space Telescope Rescue
        - Autonomous rendezvous & capture of tumbling target (chaotic, uncooperative), characterized by hypothesized saving of HST nearing its end of life
        - NASA synthetic neural system code (c/o Dr. M. Rilee @ GSFC) for autonomous recovery is being ported & parallelized at UF for HPRC operation on DM system
      - Autonomous Disturbance Detection & Monitoring System (ADDMoS)
      - On-situ sensor processing for James Webb Space Telescope (JWST)
    - Upcoming DoD apps in space, such as:
      - High-Performance Space Surveillance
      - Operationally Responsive Space (ORS)
Dependable Multiprocessor (DM)

After ST-8 orbit in 2009, future missions for DM are envisioned featuring dozens of COTS devices (PPCs, FPGAs).
6) DARPA Study on FPGA Tools

- CHREC invited to lead new study for DARPA (Sept-June)
  - Focus on R&D challenges for application development & execution on FPGA-based systems
  - Several activities
    - Identify taxonomy of tools & DOD use cases (HPC, HPEC, other)
    - Characterize limitations of existing tools, analyze technical challenges, & identify potential solutions
    - Explore & devise roadmap for future solutions & projected impact
    - Host workshop in 2008 to foster broader research discussion
  - Soliciting broad input

Creating a Research Agenda for FPGA Tools (CRAFT)

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<th>I. Formulation</th>
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<tbody>
<tr>
<td>(a) Algorithm design exploration</td>
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<td>(b) Architecture design exploration</td>
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<td>(c) Performance prediction (speed, area, etc.)</td>
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<th>II. Design</th>
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<tr>
<td>(a) Linguistic design semantics and syntax</td>
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<td>(b) Graphical design semantics and syntax</td>
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<td>(c) Hardware/software codesign</td>
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<th>III. Translation</th>
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<tr>
<td>(a) Compilation</td>
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<tr>
<td>(b) Libraries and linkage</td>
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<tr>
<td>(c) Technology mapping (synthesis, place &amp; route)</td>
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<th>IV. Execution</th>
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<tr>
<td>(a) Test, debug, and verification</td>
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<tr>
<td>(b) Performance analysis and optimization</td>
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<td>(c) Run-time services</td>
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Conclusions
Conclusions

- HPRC making inroads in ever-broadening areas
  - HPC and HPEC; from satellites to supercomputers!

- Currently, adopters are the brave at heart
  - Face weaknesses of design methods, tools, systems, devices, etc.
  - Fragmented technologies with gaps and proprietary limitations

- Research & technology challenges abound
  - Many R&D challenges lie ahead to realize full potential
  - Balancing the four Ps: performance, productivity, portability, precision

- Industry/university collaboration is critical to meet challenges
  - Incremental, evolutionary advances will *not* lead to ultimate success
  - Researchers must take more risks, explore & solve tough problems
  - Industry & government as partners, catalysts, tech-transfer recipients
Thanks for Listening! 😊

For more info:
- www.chrec.org
- george@chrec.org

Questions?

Under the auspices of the highly acclaimed program for Industry/University Cooperative Research Centers (I/UCRC) at the National Science Foundation, CHREC (pronounced "chrec") is a new national center and consortium for fundamental research in reconfigurable computing. CHREC is comprised of more than two-dozen (and growing) organizations from academia, industry, and government with synergistic interests and goals in this field. Having recently completed a two-year development, review, and selection process at NSF, CHREC became operational in January 2007. The lead academic institution for CHREC is the University of Florida, with partner institutions at George Washington University, and partner institutions at Brigham Young University and Virginia Tech. Industry and government research partners are of vital importance in CHREC, which features 21 founding members in CY2007 (listed below in alphabetical order):

<table>
<thead>
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<th>Founding Members in CHREC</th>
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<tr>
<td>AFRL</td>
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<tr>
<td>Cadence</td>
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<tr>
<td>IBM Research</td>
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<tr>
<td>NASA Langley</td>
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<td>NRO</td>
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<td>ONR</td>
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<td>SSL</td>
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A broad range of goals have been defined with NSF for CHREC, including: (1) Establish the nation’s first multidisciplinary research center in reconfigurable high-performance computing as a basis for long-term partnership and collaboration amongst industry, academia, and government; (2) Directly support the research needs of industry and government partners in a cost-effective manner with pooled, leveraged resources and minimized synergy; (3) Enhance the educational experience for a diverse set of high-quality graduate and undergraduate students; and (4) Advance the knowledge and technologies in this emerging field and ensure relevance of the research with rapid and effective technology transfer.