A New Electronic System Level Methodology for Complex Chip Designs

Chad Spackman
President, Co-Founder
We are an EDA Tool Company:

**C2R Compiler™**

- General purpose ANSI C-based design tool and flow
- Overcomes constraints of RTL design for small and large scale, complex algorithms
- Unlimited, flexible architecture exploration
- 95% of functional verification in C with standard C test tools

We are an IP Company:

**CebalIP™ CORES**

- High value IP for HW acceleration of communication, storage applications
  - GZIP compression/decompression – 1Gbps- 10Gbps available today
  - TCP/IP - 4Q2007/2008

We are a services company:

**CebalIP™ Design Services**

- Customized CebalIP features for customer applications
What sets CebaTech's C2R Compiler™ Apart?

- TRUE ANSI C Compiler
  - Pointers & pointer math
  - Function calls with arguments
  - Global variables
  - Arrays, structures, and unions
  - Looping with loop unrolling and pipelining

- INNOVATION in C-to-RTL Compilation Technology
  - Finite state machines defined by Processes
  - Hardware architecture /parallelism imposed “non-intrusively” via Compiler Directives
  - Inter-module communication via generic Interface Functions (shared I/F’s with arbitration, etc.)
  - Memory and 3Rd party IP interfaces via Accessor Functions
  - Explicit hardware mapping (WYSIWYG)

- Tool Philosophy: Architect/designer defines macro (system) architecture
  - Designer has explicit control over hardware architecture in the C source; compiler produces micro-architecture
  - Degree of concurrency (# of processes) is a design choice not imposed by compiler
  - Data path– Accomplished through C coding, not imposed by compiler
  - Compiler produces micro-architecture:
  - RTL co-simulation support
What Sets CebaTech’s C2R Compiler™ Apart?

- Validate hardware design with standard C compiler/C development environment
  - Native “C” executes faster than RTL event-based simulation, SystemC simulation
    - $10^5$ times faster than simulation
    - $10^4$ times faster in cycle accurate mode
  - Enables rapid exploration of architecture and functional test of design
  - Addresses the RTL simulation bottleneck

- Integrates with industry standard FPGA and ASIC RTL flows
  - Synthesizable RTL output
  - Readable “RTL”

**C2R Compiler™:** the first ESL behavioral synthesis tool to efficiently support **full-chip** designs
C2R Compiler R1 Development Flow

New Design In ‘C’

Existing ANSI C

“Restructure” Define HW Arch.

Structured C Source

C2R Compiler

Verilog RTL

RTL Simulation

FPGA/ASIC Synthesis FPGA/ASIC Timing FPGA Mapping/ASIC Place & Route

ASIC / FPGA Libraries

ASIC / FPGA Netlist

Compile with std C tools Test in native C environment Pseudo-cycle accurate

Verification Here
C2R Compiler R2 Development Flow

New Design In ‘C’

Existing ANSI C

“Restructure” Define HW Arch.

Structured C Source

Compile with std C tools Test in native C environment Pseudo-cycle accurate

CAC Cycle Accurate C

Compile with std C tools Test in native C environment Cycle accurate

C2R Compiler

Verilog RTL

ASIC / FPGA Libraries

FPGA/ASIC Synthesis FPGA/ASIC Timing FPGA Mapping/ASIC Place & Route

ASIC / FPGA Netlist

Verification Here

CebaTech
Summary: Benefits of CebaTech C2R™ Compiler

- **Leverage existing and Open Source software**
  - Robust, working code bases

- **Unbounded design size and complexity – SOC development capability**

- **Productivity Gains:**
  - design time
  - tool cost,
  - test coverage,
  - quality