Intel® QuickAssist Technology
Enabled FSB-FPGA Application
Accelerators

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Agenda

• Accelerators - Open Attach Strategy.
• Intel® QuickAssist Technology Enabled FSB-FPGA Accelerators - Overview and Targeted Availability
• Intel® QuickAssist Technology Accelerator Abstraction Layer
• Intel® Commitment
Intel® QuickAssist Technology

Encompasses Industry Hardware Solutions

Future Intel Processor Integration of Accelerators

Software Architecture Abstraction Layer and Libraries For Acceleration

Comprehensive Approach To Acceleration
1. Open Ubiquitous Standards Based Approach PCIe* Gen1, PCIe* Gen2, and Geneseo – (Extend PCI Express* Gen 2 - Joint Intel/IBM Proposal in PCI-SIG)

2. Enable third party FSB-FPGA Modules – targeted for FSI, Oil and Gas, Life Sciences, Digital Health, etc
   FSB-FPGA Modules Targeted 4Q07/1Q08

3. Intel® QuickAssist Technology Accelerator Abstraction Layer that seamlessly allows the SW to access acceleration across various technologies.

Open Standards Based Attach Strategy

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Why FPGA Application Acceleration

Financial Services

- Black Scholes
- Single FPGA implementation
- 11.7 GFLOPS sustained | 15 WATTS
- x18 performance of an Intel Woodcrest

Geoscience

- Kirchhoff Time Migration Algorithm
- Multi-FPGA implementation
- 40 GFLOPS sustained | 50 WATTS
- x68 performance of a 2GHz Intel Pentium-IV

Image Processing

- 3D Medical Imaging
- Single FPGA implementation
- 10 GFLOPS mixed precision sustained | 25 WATTS
- x10 performance of a 3GHz Intel Pentium-IV

All stated performance improvements are system level

Higher Performance, and Lower Power
What are FSB-FPGA Accelerators

- FPGA Modules that are plugged into a socket by replacing an Intel® Xeon® Processor and communicate using the Front Side Bus (FSB) Protocol.

![Diagram of FSB-FPGA Accelerators](Image)
Why Tightly Coupled FSB-FPGA Accelerators

- Higher Bandwidth
- Lower Latency

<table>
<thead>
<tr>
<th>Attach</th>
<th>Theoretical Peak Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSB</td>
<td>8.5GB/s @1066 MHz</td>
</tr>
<tr>
<td>PCIe* Gen 1 X8</td>
<td>4 GB/s Total (Max 2 GB/s one way)</td>
</tr>
<tr>
<td>PCIe* Gen 2 X8</td>
<td>8 GB/s Total (Max 4 GB/s one way)</td>
</tr>
</tbody>
</table>

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Higher Bandwidth and Lower latency
# Targeted Availability

<table>
<thead>
<tr>
<th>Target Availability Date</th>
<th>Platform</th>
<th>Targeted FSB-Speeds</th>
<th>System Memory Usability</th>
<th>Socket</th>
</tr>
</thead>
<tbody>
<tr>
<td>4Q07/1Q08</td>
<td>DP</td>
<td>1066 MHZ</td>
<td>Yes</td>
<td>LGA 771</td>
</tr>
<tr>
<td>4Q07/1Q08</td>
<td>MP-Caneland</td>
<td>1066 MHZ</td>
<td>Yes</td>
<td>mPGA 604</td>
</tr>
</tbody>
</table>

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Eco-System Support

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**Intel® QuickAssist Technology Accelerator Abstraction Layer (AAL)**

**Market Verticals**
- FSI
- OIL and GAS
- LIFE SCIENCES
- DIGITAL HEALTH
- HPC
- EDA
- EMBEDDED
- GENERAL ENTERPRISE

**Application(s)**

**Libraries**
MKL, IPP, Accelerator Specific, ...

**Accelerators**
e.g.: Crypto, FPGAs, XML etc

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Intel® Commitment

• Provide Validated FSB-RTL and drivers to FPGA Vendors with design guidelines (socket, board, bios, etc) for MP and DP Platforms.
• Provide Intel® QuickAssist Technology Accelerator Abstraction layer along with drivers to enable seamless SW Development and Deployment.
• Work with third party board vendors and FPGA tool providers
• Work with interested OEMs on support for FSB-FPGA solutions

We are committed to Accelerators
Summary

- Intel working to improve accelerator interface via Open Industry standard extensions to PCI Express* (Geneseo)

- Intel® QuickAssist Technology Enabled FSB-FPGA Accelerator Modules for tightly coupled attachment targeted to be available from Third Party Vendors in the 4Q07/1Q08 timeframe for MP and DP Systems.

- We are providing the Intel® QuickAssist Technology Accelerator Abstraction layer to enable customers to support accelerators.

- Intel is investing to make sure that the industry can innovate on Intel Platforms.

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Backup Slides
ANSI-C → Executable Toolflow

Source: Nallatech Ltd

- Optimize code to extract maximum parallelism
- The Nallatech application development environment supports the Industry’s most popular C-to-FPGA compiler tools:
  - DIME-C
  - Impulse-C
  - Mitrion-C

ANSI-C User Application Code → HPC Design Flow → C-to-FPGA Compilation → Application Builder → User Application running on FPGA

Intel Processors running Windows or Linux OS → Server/Blade → Software API → Xilinx ISE Implementation Tools → Runetime [Linux or Microsoft Windows Environment]

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Source: Nallatech Ltd

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HLL Design Flow
Source : XtremeData, Inc.

C Source Code

Inner Loop

Single and double-precision IEEE 754 floating-point arithmetic supported in FPGA (XDI Library) and automatically inferred from code

Compile C to HDL

Make script-driven calls to Altera tools

All Components Connected via Avalon Fabric

All RTL for FPGA
Complete Altera Project Files

Main Loop

Impulse
C Module

XDI Local Memory Interface

Intel FSB Interface

Intel®
5000P chipset

FSB at 1066 Mhz,
~ 8.5 GB/s

No user-supplied HDL source code required