Intel® QuickAssist Technology Enabled FSB-FPGA Application Accelerators

Dr. Nash Palaniswamy
Accelerator Strategy and Marketing
Server Product Group Marketing - DEG

Legal Disclaimer

- INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL® PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. INTEL PRODUCTS ARE NOT INTENDED FOR USE IN MEDICAL, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS.
- Intel may make changes to specifications and product descriptions at any time, without notice.
- All products, dates, and figures specified are preliminary based on current expectations, and are subject to change without notice.
- Intel, processors, chipsets, and desktop boards may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are available on request.
- Intel, Intel 64, Intel Leap Ahead, and the Intel logo, Intel 64 logo, Intel Leap Ahead logo, are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.
- *Other names and brands may be claimed as the property of others.
- Copyright © 2006 Intel Corporation.
- Performance tests and ratings are measured using specific computer systems and/or components and reflect the approximate performance of Intel products as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance. Buyers should consult other sources of information to evaluate the performance of systems or components they are considering purchasing. For more information on performance tests and on the performance of Intel products, visit Intel Performance Benchmark Limitations (http://www.intel.com/performance/resources/limits.htm).

Agenda

- Accelerators - Open Attach Strategy.
- Intel® QuickAssist Technology Enabled FSB-FPGA Accelerators - Overview and Targeted Availability
- Intel® QuickAssist Technology Accelerator Abstraction Layer
- Intel® Commitment

Intel® QuickAssist Technology

Encompasses Industry Hardware Solutions

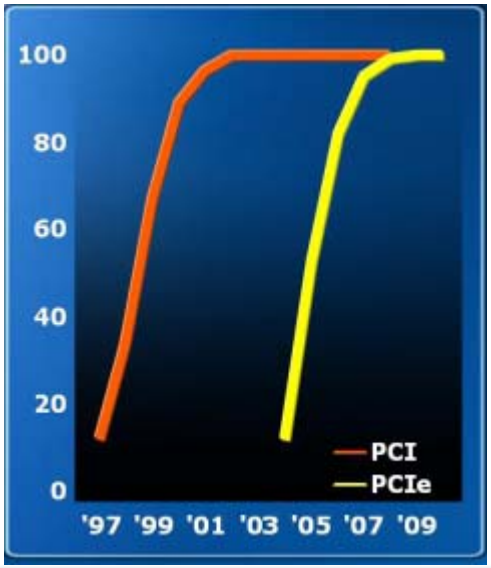
Future Intel Processor Integration of Accelerators

Software Architecture Abstraction Layer and Libraries For Acceleration

Comprehensive Approach To Acceleration

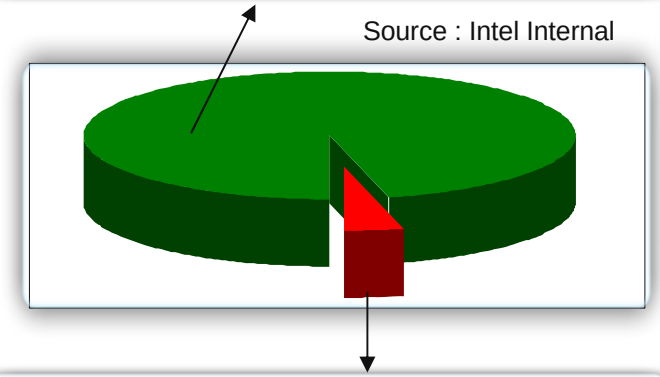
Accelerators – Open Attach Strategy

Source : Pat Gelsinger Keynote Fall IDF 2006



Geneseo – PCI Express*

Source : Intel Internal



Tightly Coupled

1. **Open Ubiquitous Standards Based Approach PCIe* Gen1, PCIe* Gen2, and Geneseo – (Extend PCI Express* Gen 2 - Joint Intel/IBM Proposal in PCI-SIG)**
2. **Enable third party FSB-FPGA Modules – targeted for FSI, Oil and Gas, Life Sciences, Digital Health, etc**

   FSB-FPGA Modules Targeted 4Q07/1Q08


3. **Intel® QuickAssist Technology Accelerator Abstraction Layer that seamlessly allows the SW to access acceleration across various technologies.**

Open Standards Based Attach Strategy

*Other names and brands may be claimed as the property of others

Why FPGA Application Acceleration

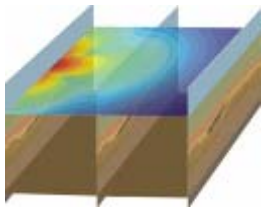
Financial Services

- Black Scholes
- Single FPGA implementation
- 11.7 GFLOPS sustained | 15 WATTS
- x18 performance of an Intel Woodcrest

NALLATECH
The High Performance FPGA Solutions Company

Source : Nallatech Ltd.

Geoscience



- Kirchhoff Time Migration Algorithm
- Multi-FPGA implementation
- 40 GFLOPS sustained | 50 WATTS
- x68 performance of a 2GHz Intel Pentium-IV

Image Processing

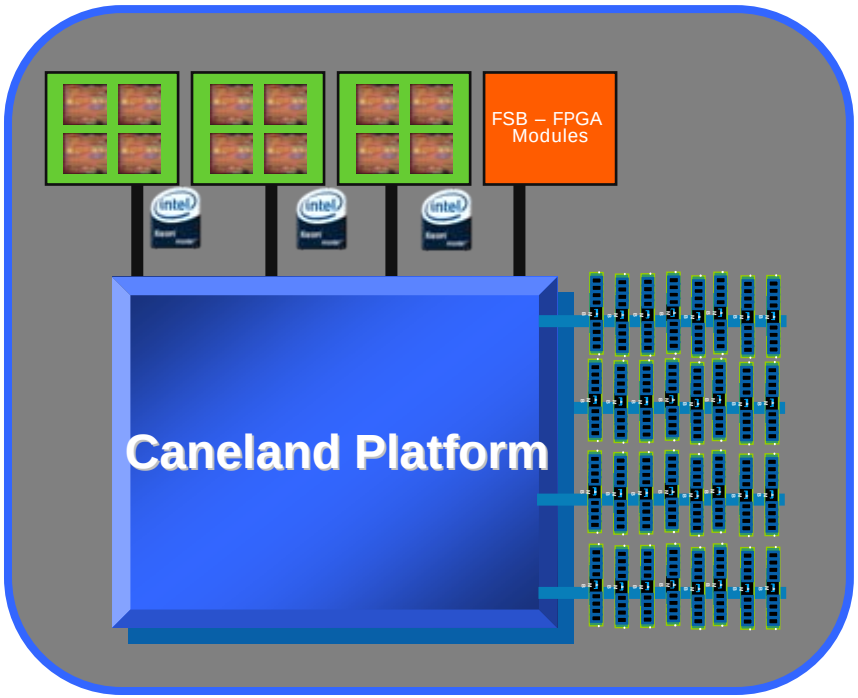
- 3D Medical Imaging
- Single FPGA implementation
- 10 GFLOPS mixed precision sustained | 25 WATTS
- x10 performance of a 3GHz Intel Pentium-IV

All stated performance improvements are system level

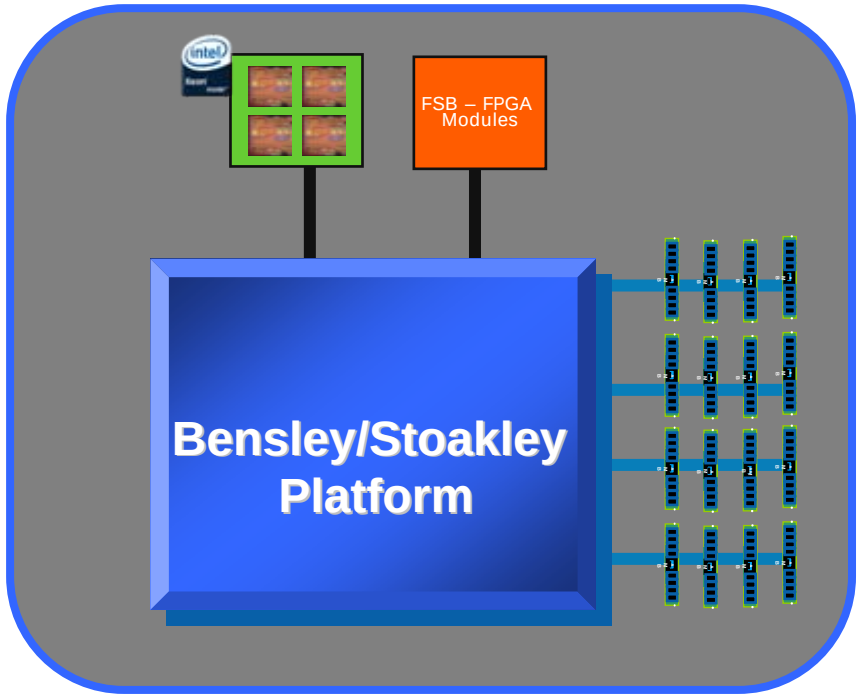
Higher Performance, and Lower Power

What are FSB-FPGA Accelerators

- FPGA Modules that are plugged into a socket by replacing a Intel® Xeon® Processor and communicate using the Front Side Bus (FSB) Protocol.



7000 Sequence



5000 Sequence

Why Tightly Coupled FSB-FPGA Accelerators

- Higher Bandwidth
- Lower Latency

Attach	Theoretical Peak Bandwidth
FSB	8.5GB/s @1066 MHz
PCIe* Gen 1 X8	4 GB/s Total (Max 2 GB/s one way)
PCIe* Gen 2 X8	8 GB/s Total (Max 4 GB/s one way)

Higher Bandwidth and Lower latency

*Other names and brands may be claimed as the property of others

Targeted Availability

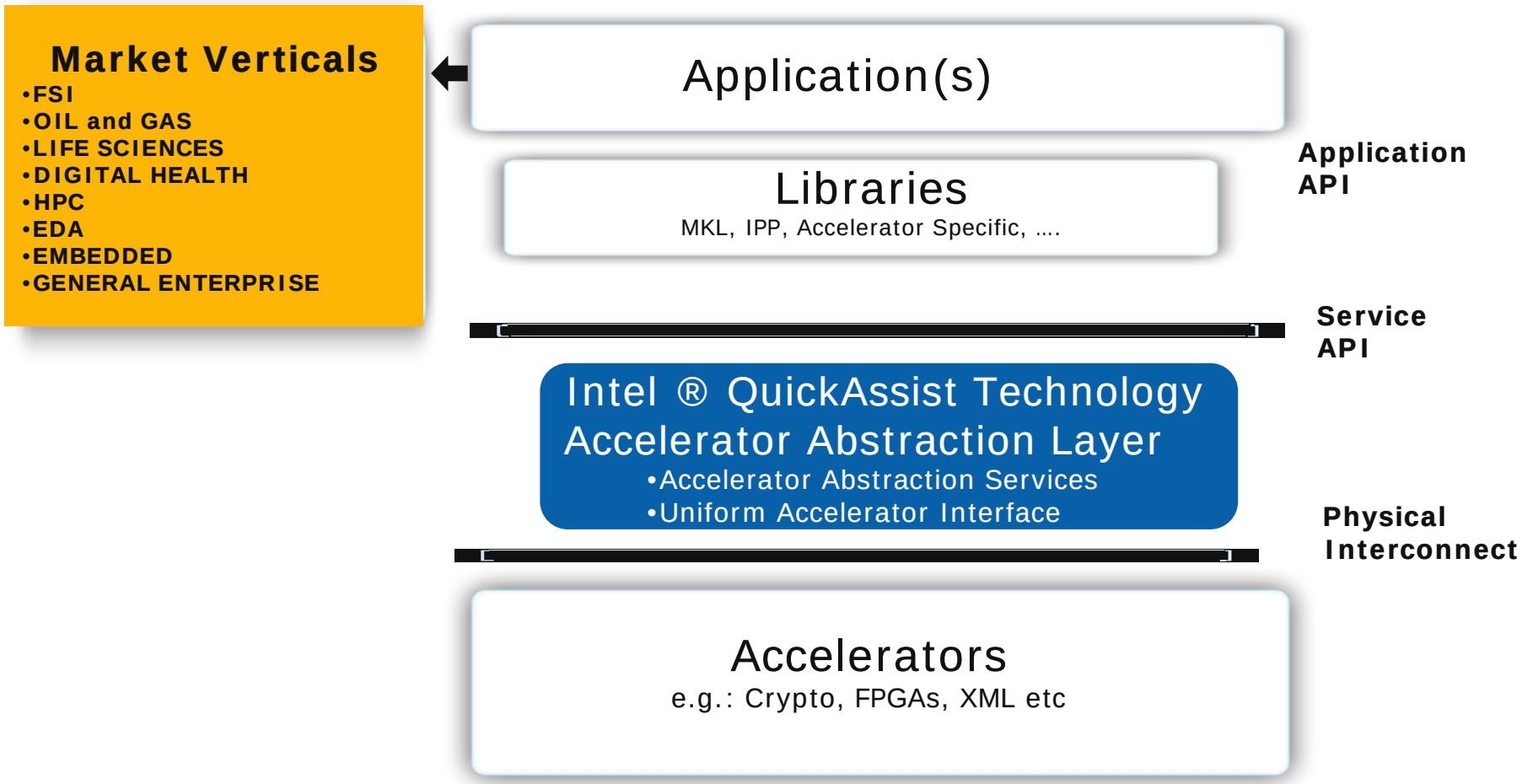
Target Availability Date	Platform	Targeted FSB-Speeds	System Memory Usability	Socket
4Q07/1Q08	DP	1066 MHZ	Yes	LGA 771
4Q07/1Q08	MP-Caneland	1066 MHZ	Yes	mPGA 604

*Other names and brands may be claimed as the property of others

Eco-System Support

*Other names and brands may be claimed as the property of others

Intel® QuickAssist Technology Accelerator Abstraction Layer (AAL)



*Other names and brands may be claimed as the property of others

Intel® Commitment

- Provide Validated FSB-RTL and drivers to FPGA Vendors with design guidelines (socket, board, bios, etc) for MP and DP Platforms.
- Provide Intel® QuickAssist Technology Accelerator Abstraction layer along with drivers to enable seamless SW Development and Deployment.
- Work with third party board vendors and FPGA tool providers
- Work with interested OEMs on support for FSB-FPGA solutions

We are committed to Accelerators

Summary

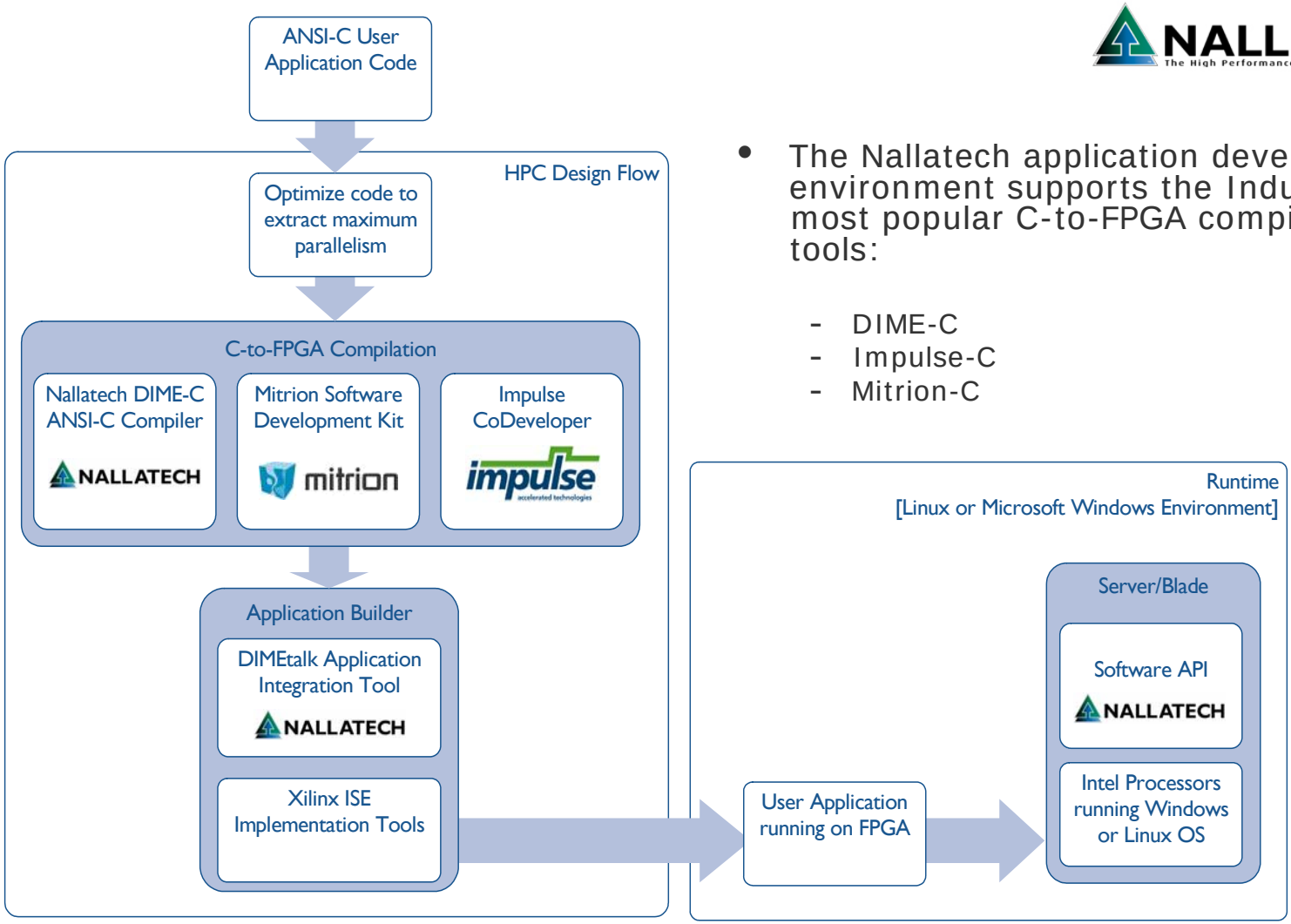
- Intel working to improve accelerator interface via **Open Industry standard extensions to PCI Express* (Geneseo)**
- **Intel® QuickAssist Technology Enabled FSB-FPGA Accelerator Modules** for tightly coupled attachment targeted to be available **from Third Party Vendors in the 4Q07/1Q08 timeframe for MP and DP Systems**.
- We are providing the **Intel® QuickAssist Technology Accelerator Abstraction layer** to enable customers to support accelerators.
- Intel is investing to make sure that the **industry can innovate on Intel Platforms.**

*Other names and brands may be claimed as the property of others

Backup Slides

ANSI-C → Executable Toolflow

Source: Nallatech Ltd



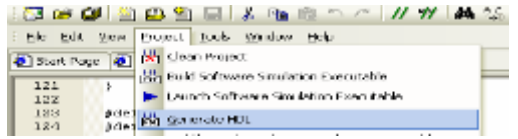
- The Nallatech application development environment supports the Industry's most popular C-to-FPGA compiler tools:
  - DIME-C
  - Impulse-C
  - Mitrion-C

HLL Design Flow
Source : XtremeData, Inc.

C Source Code

Inner Loop

Single and double-precision IEEE 754 floating-point arithmetic supported in FPGA (XDI Library) and automatically inferred from code



Compile C to HDL

Main Loop

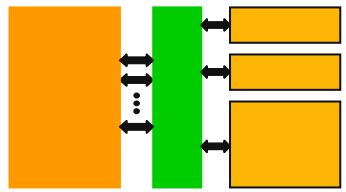
Impulse C Module

XDI Local Memory Interface

Intel FSB Interface

SOPC Builder

All Components Connected via Avalon Fabric



Make script-driven calls to Altera tools

FSB at 1066 Mhz, ~ 8.5 GB/s

Intel®
5000P chipset
intel

FSB at 1066 Mhz, ~ 8.5 GB/s

All RTL for FPGA

Complete Altera Project Files

No user-supplied HDLsource code required