SRC Computers
2007 and Beyond
July 19, 2007
Present
**IMPLICIT+EXPLICIT™ Architecture**

- SRC is about a hardware and software architecture
- Peer relationship to all resources is key

- **Implicitly Controlled Device**
  - Dense logic device
  - Typically fixed logic
  - μP, DSP, ASIC, etc.

- **Explicitly Controlled Device**
  - Direct execution logic
  - Typically reconfigurable
  - FPGA, CPLD, OPLD, etc.

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**Carte™ Programming Environment**

- Fortran

**Unified Executable**

- Memory Control
- Memory
- I/O Bridge
SRC’s Unique Position

• Control over Hardware and Software design uniquely positions SRC

• Carte™ C and Fortran programming environment is optimized for a particular hardware resource mix

• MAP® Hardware resource mix is altered to simplify programming environment

• Carte allows ANSI C and Fortran application development for systems with multiple μP and FPGAs

• Robust debug capability
  – Accurate performance prediction for complete systems
  – Feedback on pipelinability
  – Debug application like a programmer at normal debug speeds
SRC-6 Product Line

- SRC-6 product line will continue
  - New SRC-6 systems are still being deployed
  - Will support existing system expansion as long as demanded
  - Will support “like system” additions as long as demanded
SRC-6 Embedded Servers

- Multi-MAP switch based systems are now being integrated as an embedded system in new designs.
SRC-7 Now Shipping

• Two MAPstations shipped to USC
  – 2U MAPstations with Series H MAP
  – Initially used to continue MPI efforts using heterogenous nodes
  – Cluster consists of 2 μP nodes and 2 μP with MAP nodes
  – Existing SRC-6 nodes may be added to the cluster

• First multi-MAP MAPstation in test for NCSA
  – Tower with 6 port Hi-Bar switch, 2 CM banks & 2 Series H MAPs
  – Used to continue current efforts on a variety of applications
  – Allows multi-MAP applications
SRC-7 Remaining Efforts

- **16 port Hi-Bar switch**
  - First switches are built
  - Testing has started and will get underway in earnest in August
  - Expect to be able to ship systems in Q4-2007

- **Continued system enhancements**
  - As with SRC-6, FPGAs throughout system allow for continual hardware feature updates
  - Customer feedback will provide MANY opportunities to improve
Series H MAP®

- 1 or 2 LVDS main I/O ports
- 4 simultaneous input and output DMAs
- 150 MHz nominal User Logic speed
- 16 simultaneous SRAM OBM references
  - SDRAM a possibility
- 2 dedicated 64 bit Bridge Ports
- 2 simultaneously accessible DDR2 SDRAM OBCM banks
  - Initial release is 512 MB, 1 GB to follow
- GPIO eXpansion (GPIOX) cards

MAP

- 8 Banks On-Board Memory (64 MB SRAM)
- 4.2 GB/s
- 4.2 GB/s
- 14.4 GB/s sustained payload (7.2 GB/s per pair)
- 12 GB/s GPIO

Controller

- User Logic 1
  - 55 Mgates
  - 4.8 GB/s
- User Logic 2
  - 55 Mgates
  - 4.2 GB/s

SDRAM

- 1 GB
- 2 banks

Eight Banks On-Board Memory (64 MB SRAM)

19.2 GB/s (2.4 x8)

5.25" Drive Bay Enclosure
SRC-7 MAPstation™

- Two 4.2 GB/s Common Memory banks integrated into Hi-Bar
- Up to 3 MAPs (each with GPIOX & 2 CM banks) in single tower
- Single MAP systems do not require Hi-Bar, available in 2U
SRC-7 Hi-Bar® Based Systems

- Hi-Bar sustains 3.6 GB/s payload per path with 180 ns latency per tier
- 2 tiers support 256 nodes
- MAP can use 1 or 2 Hi-Bar ports
- GPIO can be chained or used for direct data input to MAP
- High bandwidth disks connect directly to switch
Impact of Altera on Performance

- Total Local Memory
- OBM SRAM Size
- User Logic M gates
- Sustained GPIO Payload BW
- SPFP Perf
- DPFP Perf
- OBM SRAM BW
- SRC-6 Series E
- SRC-6 Series C

- 60 M gates
- 28 MB
- 2.4 GB/s
- 4.8 GB/s
- 6.4 Gbytes/s
- 24 GF
- 10 GF
- 2.4 GB/s
- 4.8 GB/s
Impact of Altera on Performance

- User Logic Mgates: 110 Mgates (359K LUT/FF)
- Total Local Memory: 2048 MB
- OBM SRAM Size
- 70 GF SPFP Perf
- 35 GF DPFP Perf
- 14.4 GB/s Sustained Interface Payload BW
- 12 GB/s Sustained GPIO Payload BW
- 19.2 GB/s User Logic OBM SRAM BW
- SRC-6 Series C
- SRC-6 Series E
- SRC-7 Altera Based
Near Future
High Bandwidth Disk

• Removes the last major barriers to peer operation
• Sustained disk bandwidth equal to Hi-Bar port
• Looks like large common memory
• First customer order received
  – Targets an SRC-6 system
  – 10K uncached random IOPs per assembly
  – 14 Tbytes per assembly
  – Saturates Hi-Bar during sequential or cached accesses
  – 3 year sealed fail in place operation
  – Delivery in November of 2007
• Controller will gain Complex DMA capability
  – Scatter/gather, array merge, etc
Series I MAP

- Customer inputs requested a reduced capability MAP
  - Generally used for streaming applications
  - Maintains Carte programming environment
  - Much lower price point

- The Series I MAP is in response to this
- Combines SNAP and MAP into one module
- Will also be available as a module product for existing system retrofit or OEMs
Series I MAP

- Works in Intel or AMD motherboard DIMM slots
- mP uses SDRAM on SNAP just as other DIMMs
- When SNAP has control of its SDRAM mP continues to use SDRAM DIMMs effectively doubling memory BW

**Memory Controller in Bridge or µP**

**SDRAM**

**Motherboard SDRAM DIMMs**

**Motherboard SDRAM DIMMs**

**Isolation Switches**

**SNAP & Control**

**User Logic**

**SRAM**

**Altera EP2S180**
- 166 MHz nominal clock
- ‘S130 or ‘S90 stuffing options

**Altera EP2S90**
- Interface to DIMMs
- DMA Engine
- Reconfiguration control
- Eliminates any chance of bad user design loosing communications to MAP

**4MByte QDR SRAM**
- Read/modify/write without slowdown
- Stuffing option to delete

**DDR 333 SDRAM**
- Two .5GB or 1GB DIMMS Accessible by µP or MAP
- Moving to DDR2 533 late ‘07
Multi-Core Processors

• Some customers have interest in multi-core processors
  – Difficult to program
  – Do benefit some applications quite well
  – Very high power consumption
  – Limited interconnect topology options

• SRC is evaluating incorporation of such processors

• SRC has the ability to solve many of the issues
  – Carte already deals with highly parallel processors
  – SRC mechanical systems already handle very high power level
  – SRC systems can accommodate these processors in cluster, crossbar switch and MAP GPIO topologies
  – Any number could be incorporated into a system

• Consistent with SRC’s IMPLICIT+EXPLICIT Architecture
Multi-core processors are just another implicit device.

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Portability

• As the first step in achieving portability SRC wants to have MAP and Carte available on all major μP brands
  – 2 of 3 already accomplished

• SRC may also entertain putting Carte on non-SRC platforms in markets where we do not see a MAP play
  – This must be balanced with business needs

• MAP may become available from other sources
Future View of Hardware

• **IMPLICIT+EXPLICIT** Architecture will continue
  – Peer coupling of heterogenous processors

• FPGAs will remain the dominant EXPLICIT device
  – Only product with enough market share to justify costs

• New IMPLICIT devices will be used
  – Most likely a multi-core device
  – Some of those cores will be graphics processor

• **Packaging**
  – Stacked die will become the norm
  – MAP and μP will exist in a single package
Future View of Software

“I don’t know what it will look like but it will be called Fortran”

S. Cray

- “New” languages not expected to dominate
- Extensions to existing standard languages are expected
- Carte may become available on non-SRC products
  - Business case dependant
Future Use

- Reconfigurable devices are much like separate floating point processors were in the 80s
- Heterogeneous systems will be in general purpose
  - Stacked die packages will make this economical