Performance Analysis of SGI RASC RC100 Blade on 1-D DWT

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Motivation

- Wide gap between Theoretical Performance projection and Actual Performance on FPGA hardware

For e.g. the theoretical throughput of a 1-D DWT Algorithm Block on FPGA

8 Pixels / clock Cycle, 200MHz Design = 1.6 Giga Pixels/s

But, the Actual throughput on RC100 blade is 0.9 Giga Pixels/s

- Acceleration on FPGA is limited by the bandwidth of the I/O interface that connects it to the host system
Data Flow in the RC 100 Blade

ASIC connecting FPGA to external System via NUMAlink

Core Services

Algorithm

Virtex-4 LX 200

Data Flow in the RC 100 Blade

- 3.2 GB/s @ 200MHz
- 16MB

Algorithm

- 3.2 GB/s @ 200MHz
- 16MB
Interface Throughput of RC100

I/O Throughput Chart of the Virtex 4 LX 200 FPGA on RC 100

Throughput (Megabytes / sec)

Data Sent / Received

Direct I/O (Mbytes/s)
Buffered I/O (Mbytes/s)
Streaming I/O (Mbytes/s)
Implementing 1-D DWT on FPGA

Direct/Buffered I/O

Image From Host via NUMALink

128

MEM 1

128

1-D DWT Block

128

MEM 0

128

DWT to Host via NUMALink

OR

Streaming I/O

Image From Host via NUMALink

128

1-D DWT Block

128

DWT to Host via NUMALink
Tool Flow

1-D 5-3 DWT Algorithm from OpenJPEG Library

Compiled Through ROCCC

VHDL with Core-Services Synthesized and Implemented using XST, PAR

Bitstream Loaded with devmgr

Bitstream Loaded with devmgr

C source

VHDL code

Bitstream

Benchmarks run
for (i=0; i<LEN; i=i+4) {
    Lift1_2 = a[i+1] - (a[i]+a[i+2])/2;
    Lift1_3 = a[i+3] - (a[i+2]+a[i+4])/2;
    Lift2_1 = a[i] + (Lift1_2 + Lift1_1 + 2)/4;
    Lift2_2 = a[i+2] + (Lift1_2 + Lift1_3 + 2)/4;
    Lift1_1 = Lift1_3;
    b[i] = Lift1_2;
    b[i+1] = Lift1_3;
    b[i+ROW/2] = Lift2_1;
    b[i+1+ROW/2] = Lift2_2;
}

Riverside Optimizing Compiler for Configurable Computing
Pipeline generated by ROCCC

Stage 1 Processing

Stage 2 Processing

Data_In[n] Data_In[n+1]

Data_Out[n-1] Data_Out[n]
Performance of 1-D 5-3 DWT

Data Throughput of the 1-D DWT Algorithm on the SGI Altix 4700

Throughput (Mega Pixels / sec)

Source Image Component Size (Mega Pixels) [16-Bit / Pixel]

- RC100 using (Direct IO)
- RC100 using (Streaming IO)
- OpenJPEG on Itanium2 (1.6 GHz) Intel C Compiler