MP3 decoding on FPGA: a case study for floating point acceleration

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Motivation: Explore acceleration of applications based on Floating-Point arithmetic using an Application Specific Instruction-set Processor (ASIP) paradigm.
Achieved a **33% speedup** over a NIOS2 processor with FP extensions by applying the CIs to the most critical application function.

Explored the design and use of CI accelerators with **wider bitwidth** (DPFP) than the processor.