Radio Astronomy Signal Processing for Pulsar Searching using High Performance Reconfigurable Computers

Don Backer
Center for Astronomy Signal Processing and Electronics Research, and Department of Astronomy, University of California, Berkeley

Peter McMahon
Center for Astronomy Signal Processing and Electronics Research, University of California, Berkeley
Department of Electrical Engineering, University of Cape Town

Joeri van Leeuwen
Center for Astronomy Signal Processing and Electronics Research, and Department of Astronomy, University of California, Berkeley

Dan Werthimer
Center for Astronomy Signal Processing and Electronics Research, and Space Sciences Laboratory, University of California, Berkeley

Abstract

This poster will describe our preliminary work to use high performance reconfigurable computers to accelerate the signal processing required for performing a pulsar search on data from a radio telescope. Specifically, we are using the Berkeley Emulation Engine (BEE2) reconfigurable computer and Internet BreakOut Board (IBOB) hardware developed by the CASPER group at Berkeley, and the MATLAB/Simulink design flow. In the poster, we will show the architecture of our system, and how we use the BEE and IBOB hardware to move and process data from the outputs of a telescope right through to a 10GbE connection, which is connected to a conventional computer cluster, which performs data storage and further data processing.

1. The Berkeley Emulation Engine and Internet BreakOut Board

BEE2 [1] is a Virtex 2 Pro-based reconfigurable computer that was designed primarily to perform chip emulation and signal processing, tasks at which it excels. Each BEE2 board has five Virtex 2 Pro FPGAs, with the PowerPC core of one FPGA used to run the Linux-based operating system, "BORPH". Each FPGA has up to 8GB of memory, and the board has 18 10Gbit/s I/O connections, which can implement 10GbE and use standard 10Gb Ethernet switch hardware. This makes the BEE2 platform a powerful general purpose reconfigurable computing platform.

The IBOB is a generic I/O module that can be connected to the BEE2 board by high-speed serial links. Its principle purpose in the context of our project is, in conjunction with an Analog-to-Digital Converter (ADC) board, to supply the BEE2 reconfigurable computer with a stream of digitized data to process.

2. Pulsar Search and Radio Astronomy Signal Processing

Pulsars are rapidly rotating astronomical objects that emit electromagnetic radiation that can be detected by radio telescopes on Earth. The signals from pulsars appear as periodic pulses in received data, but due to the small amplitude of the pulses, the noise received and the effects that traveling through space to Earth have on the radiation, detecting these pulses is not trivial. The computational problem can essentially be broken into two stages: channelizing the received signal, and performing dedispersion and the Fast Folding Algorithm on the channelized data. Channelizing the data involves decomposing the received signal into a range of frequency bins. Dedispersion attempts to reverse an effect that the Interstellar Medium (ISM) has on the signal as it

travels to Earth, and the Fast Folding Algorithm is used to search for signal peaks.

Channelization for pulsar search has, in most recent radio telescope projects, been performed using specialized hardware. However, the BEE2 reconfigurable computer is an ideal platform for implementing and accelerating channelization. It has the IO and processing resources that are necessary, and the BEE2 is already being used for various other radio telescope signal processing tasks.

With regard to the dedispersion and Fast Folding Algorithm implementations, the current data rates and the resulting processing requirements are not sufficient to warrant an extensive effort to accelerate them. These tasks are typically performed on a cluster using a set of well-known and well-tested software packages. The output from the channelizer thus needs to be sent efficiently to a compute cluster that can perform these tasks.

Currently a system, the ASP [2], is used at numerous observatories, and partially performs a similar function to what we are developing. However, it uses older FPGA technology, and a custom interconnect. We want to increase the bandwidth and spectral resolution of the system by using more modern FPGAs, and use industry standard interconnect to reduce cost and increase the maintainability of the project.

3. Architecture and Implementation

We are presently designing and implementing a system with the architecture shown in Figure 1.

Data is received from the telescope and digitized by an ADC. It is then channelized on the BEE reconfigurable computer, and packetized into 10Gb/sec Ethernet packets, which are sent to a switch which as one 10GbE port, and multiple 1GbE ports. The conventional compute cluster nodes hang off the switch.

All the programming of the reconfigurable computer is done in the MATLAB/Simulink environment. Each of the blocks shown are implemented in Simulink, and can be efficiently synthesized on an FPGA. The PFB, or Polyphase Filter Bank, is the most important block in the process, and is well-suited to FPGAs as it is easily parallelizable. In the poster we will outline our Simulink design, and our results. We will also discuss the performance of the 10GbE/1GbE interface, and how data was moved from the reconfigurable computer to the cluster.

4. References

[1] C. Chang, J. Wawrzynek, and R. Brodersen, "BEE2: a high-end reconfigurable computing system", *IEEE Design and Test of Computers*, March-April 2005, pp. 114-125.

[2] P. Demorest, "Measuring the Gravitational Wave Background using Precision Pulsar Timing", Ph.D. Thesis, May 2007.

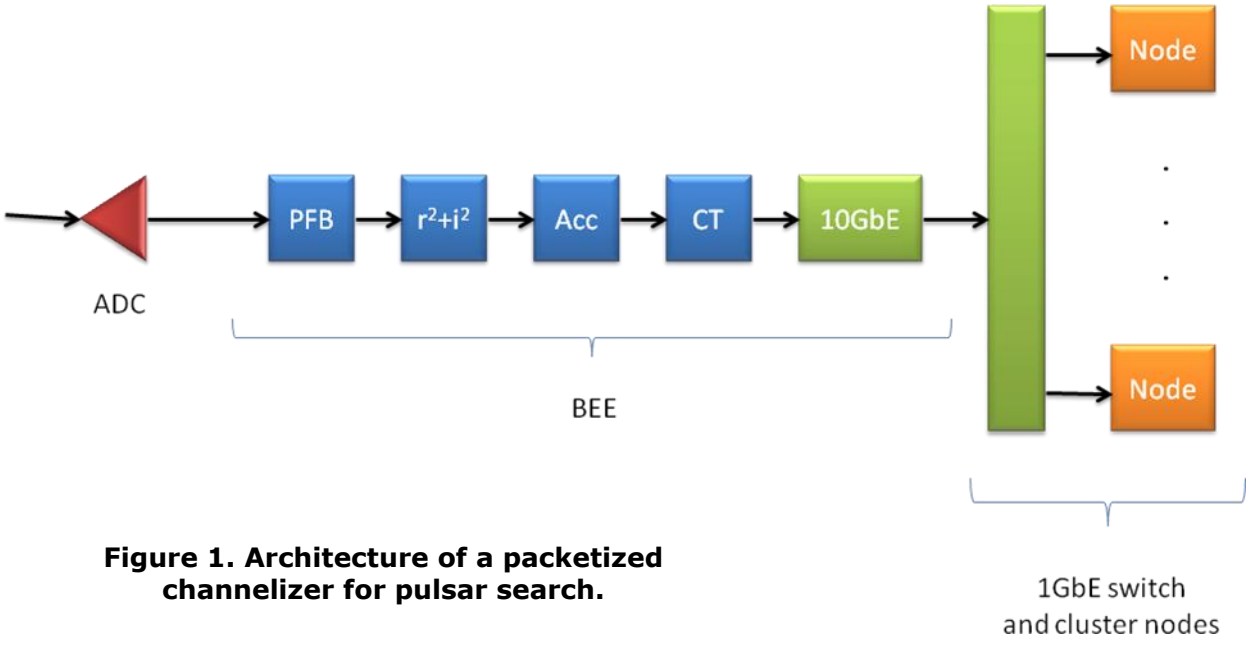

Figure 1. Architecture of a packetized channelizer for pulsar search.